Modem Portability/SDR Issues

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28 April 2004

SDR Developments at Titan CEWD

- **CEWD is developing a FPGA-based multi-purpose modem (MPM) that is being used on a Ka-Band and Ku-Band satellite-based network**
- **The MPM hosts two completely different modems that are designed for a hub-spoke network topology and a mesh-network topology**
- **Modem consists of up to 3 Xilinx Virtex - II Pro devices with 33,000 Slices each + MPC8270 processor + external DSP devices to perform digital downconversion/decimation and digital upconversion/interpolation + 70 MHz IF chain using bandpass sampling techniques**
  - **Logic synthesized to operate at 96 MHz**
  - **Qty (392) 18 x 18 multipliers /device (>200 MHz)**
  - **Embedded PPC processors**

Implementation Issues

- **FPGAs use ASIC design flow with Lower NRE cost but higher recurring costs**
  - **Bleeding-edge FPGAs around $2,000 ea. in quantity**
  - **Using FPGA flow the HDL source language is portable from device to device, with clock speed and mapping caveats**
  - **Can be more difficult to debug. Relies on test bench.**
- **DSP provides lowest NRE cost**
  - **Flexible, can be easier to debug in the target**
  - **Their generic architecture makes them non-optimal for high-bandwidth algorithms**
  - **Lower cost in general**
- **Neither DSP nor FPGA alone can meet the constraints of the entire spectrum of waveforms (power, cost, performance)**
- **On Average Price Per Gate or MIP Drops 50% Every 2 Years**

FPGA and DSP Portability

- **Coding standards, common IP blocks, design rules must be followed to allow portability**
  - **Synchronous/Asynchronous issue**
  - **Registered functional blocks (where possible) to mitigate timing/routing issues**
  - **Best practice to develop library of common functions**
    - **Reed Solomon FEC IP**
    - **CEVD IP**
    - **Turbo (SCCC, TPC) IP**
    - **Matched filter**
    - **PSK FDMA/TDMA synchronization library**
    - **MSK/CPM FDMA/TDMA synchronization library**
    - **QAM FDMA/TDMA synchronization library**
    - **OFDM synchronization library**
    - **Multirate filter library**
    - **Detection library**
    - **Equalization library (LTE, DFE, MLSE, CMA, LMS, RLS)**

DSP Portability Issues

- Language standardization
  - Compiler differences among targets
- Operating system convergence
  - Everyone has their favorite, including no-O/S
- Floating point vs. fixed point
  - Power consumption: manpack, rack-mount
  - Time to market
- DSP micro-architecture issues
  - Optimization to meet constraints reduces portability
  - Need to move to a core-based IP model?

Analog Interface Issues

- Flexible analog interfaces required or modularized approach
  - Zero IF (most compatible—lowest cost)
    - Gain/phase imbalance issues (Tx & Rx)
    - DC offset issues (Rx)
  - 70 MHz IF (industry standard)
    - Channel BWs < ~40 MHz
    - Availability of commercial market parts
  - Standard Tx power control, power sensing amplifiers
  - Rx amplifier IC with digital interface
    - TDMA must be quick interface with accurate relative gain adjustment
  - PA options for differing applications
- TX / RX switching times, frequency agility